UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/661,295	09/12/2003	Peter Poechmueller	INTECH 3.0-102 03 P 51716	7427

48154 7590 04/18/2006

SLATER & MATSIL LLP
17950 PRESTON ROAD
SUITE 1000
DALLAS, TX 75252

EXAMINER	
ROSSOSHEK, YELENA	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 04/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/661,295	POECHMUELLER, PETER	
	Examiner	Art Unit	
	Helen Rossoshek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,8-10 and 31-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6, 8-10* is/are rejected.

7)☒ Claim(s) *31-42* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the Application 10/661,295 filed 09/12/2003 and amendment filed 01/31/2006.

2. Claims 1-6, 8-10 and 31-42 are pending in the Application. Claims 7 and 11-30 have been cancelled from the Application. Claims 31-42 have been added to the Application.

3. Applicant's arguments have been fully considered but they are not persuasive.

Claim Objections

4. Claims 1, 31, 32, 35, 36, 39 and 40 are objected to because of the following informalities:

Applicant's amended term "by a predetermined incremental spacing" of the claim 1 is indefinite or uncompleted. Examiner's assumption is that a term "amount" or "value" or "constraint" is missed. New claims 31, 32, 35, 36, 39 and 40 having the same term appear with the same problem, as well as the limitation 10) of the claims 31, 35 and 39, such as "increasing the spacing".

Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States

only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-6, 8-10 are rejected under 35 U.S.C. 102(e) as being anticipated by Gopalakrishnan et al. (US Patent 6,874,133).

With respect to claims 1 Gopalakrishnan et al. teaches an automatic machine-implemented method of de-compacting a layout of a portion of an integrated circuit, within providing an automated circuit design layout compaction method (col. 1, ll.7-9, ll.59-63) with an ability of the **increasing** and/or decreasing the spacing or distance between member devices (col. 6, l.67; col. 7, ll.1-2), wherein increasing the spacing between member is performed, when a violation of spacing constraint is found as a result of compaction the layout of IC (col. 3, ll.35-47) and increasing the space between member devices is **de-compacting**, comprising: automatically (col. 6, ll.62-63) enlarging a spacing between neighboring features of a path of a layout by a predetermined incremental spacing provided that the length of the path does not then exceed a predetermined dimensional constraint and provided that connectivity is maintained between the neighboring features and any features of the layout to which the neighboring features are connected within the compaction method by increasing the distance between two member devices (col. 14, ll.13-14, ll.17-20), wherein the process of increasing the distance between two member devices is done without violation of the spacing constraints (col. 3, ll.48-52) with consideration the neighboring member devices affected by processing of increasing the distance between two member devices (col. 14, ll.66-67; col. 15, ll.1-7); and repeating the enlarging for at least one other spacing of the layout within processing increasing the distance between two member devices as show

on the Figs. 8(a) and 8(b), wherein increasing the distance is performed until the spacing constraints are met (col. 14, ll.50-53), wherein the process can be performed iteratively (col. 7, ll.38-42).

With respect to claim 10 Gopalakrishnan et al. teaches a method of de-compacting a layout of a portion of an integrated circuit within providing an automated circuit design layout compaction method (col. 1, ll.7-9, ll.59-63) with an ability of the **increasing** (de-compacting) and/or decreasing the spacing or distance between member devices (col. 6, l.67; col. 7, ll.1-2), wherein increasing the spacing between member is performed, when a violation of spacing constraint is found as a result of compaction the layout of IC (col. 3, ll.35-47) and increasing the space between member devices is **de-compacting,** comprising: a) providing a predetermined dimensional constraint for the layout in a first direction of the layout by setting the spacing constraints associated with each member device of the layout forming an integrated circuit (abstract; col. 1, ll.7-9); b) automatically enlarging a spacing between first and second features of a path of the layout by a predetermined amount, provided that the length of the path does not then exceed the predetermined dimensional constraint within the compaction method by increasing the distance between two member devices (col. 14, ll.13-14, ll.17-20), wherein the process of increasing the distance between two member devices is done without violation of the spacing constraints (col. 3, ll.48-52) and provided that connectivity is maintained between the first and second features and any features of the layout to which the first and second features are connected, when the spacing is smaller by the predetermined amount than the larger of a first neighbor

spacing between the first feature and a third feature of the path neighboring the first feature, and a second neighbor spacing between the second feature and a fourth feature of the path neighboring the second feature when the process of increasing the distance between two member devices is performed with consideration the neighboring member devices affected by processing of increasing the distance between two member devices (col. 14, ll.66-67; col. 15, ll.1-7); and c) repeating the step b) in order from a smallest the spacing enlargeable by the step b) until all spacing enlargeable by the step b) are enlarged as many times as enlargeable within processing increasing the distance between two member devices as show on the Figs. 8(a) and 8(b), wherein increasing the distance is performed until the spacing constraints are met (col. 14, ll.50-53), wherein the process can be performed iteratively (col. 7, ll.38-42).

With respect to claims 2-6, 8 and 9 Gopalakrishnan et al. teaches that:

Claim 2: enlarging is repeated until all enlargeable spacing of the layout are enlarged within processing increasing the distance between two member devices at an appropriate time until spacing constraints are met as shown on the Figs. 8(a) and 8(b) (col. 14, ll.50-53; ll.56-61);

Claim 3: spacings are enlarged in order from a smallest spacing of the layout within the compaction method including compacting and de-compacting processes are embodied in a computer software program (col. 7, ll.15-16) and might be processed in any order or simultaneously (col. 7, ll.37-41) generally depending on the computer program code when the violation of the spacing constraints is found, i.e. when as a

result of compaction the distance between two member devices does not meet spacing constraint (smaller then permitted) (col. 3, ll.44-47);

Claim 4: predetermined dimensional constraint is a critical path length (C) of the layout in a first direction of the layout (col. 15, ll.4-7, ll.16-19);

Claim 5: predetermined dimensional constraint represents a dimension of an area available for the layout in a first direction as shown on the Figs. 8(a) and 8(b) (col. 14, ll.60-65);

Claim 6: predetermined dimensional constraint limits the length of the path in a first direction of the layout, wherein the neighboring features include a first feature and a second feature neighboring the first feature of the spacing, wherein the path includes a first neighbor spacing between the first feature and a third feature neighboring the first feature, and when the path includes a fourth feature neighboring the second feature, the path further includes a second neighbor spacing between the second feature and the fourth feature, wherein the spacing is enlarged only when the spacing is smaller than the larger of the first neighbor spacing and the second neighbor spacing by a predetermined amount when the path includes the fourth feature, and when the path does not include the fourth feature, the spacing is enlarged only when the spacing is smaller than the first neighbor spacing by the predetermined amount within the process of increasing the distance between two member devices is done without violation of the spacing constraints (col. 3, ll.48-52) with consideration the neighboring member devices affected by processing of increasing the distance between two member devices (col. 14, ll.66-67; col. 15, ll.1-7);

Claim 8: the spacing is enlarged, the larger of the first neighbor spacing and the second neighbor spacing is reduced by the predetermined amount when the path includes the fourth feature, and when the path does not include the fourth feature, the first neighbor spacing is reduced by the predetermined amount within the combination of increasing and decreasing the distance between member devices (col. 15, ll.61-63) with consideration the neighboring member devices affected by processing of increasing the distance between two member devices (col. 14, ll.66-67; col. 15, ll.1-7);

Claim 9: each the spacing is enlarged as many times as enlargeable within processing increasing the distance between two member devices at an appropriate time until spacing constraints are met as shown on the Figs. 8(a) and 8(b) (col. 14, ll.50-53; ll.56-61; col. 7, ll.41-43).

Allowable Subject Matter

7. Claims 31-42 have allowable subject matter. The prior art of record does not disclose the specific arrangement of elements including the step of determining whether the actual spacing of the branch plus a predetermined incremental spacing is less than or equal to the larger of the spacing of the branch of the layout under evaluation that is previously estimated branch (predecessor) and less than or equal to the spacing of the branch under evaluation that is the successor branch, and if the spacing of the particular branch plus the predetermined incremental spacing is not less than both the spacing of the predecessor branch and the spacing of the successor branch, locking the particular branch and returning the step of determining if there is a new candidate branch for estimation; and determining whether the graph connectivity restrictions of the

layout allow the spacing of the particular branch to be increased by the predetermined incremental spacing, if the graph connectivity restrictions of the layout does not allow the spacing for the particular branch to be increased, locking the particular branch and returning to the step of determining if there is a new candidate branch for estimation.

Remarks

8. In the remarks Applicant argues in substance:

a) Gopalakrishnan et al. does not teach steps of enlarging a spacing between neighboring features of a path of the layout by a predetermined incremental spacing provided that the length of the path does not exceed a predetermined dimensional constraint; and repeating enlarging for at least one other spacing of the layout

b) Gopalakrishnan et al. does not teach enlarging a spacing until the length of a path does exceed a critical path length

c) Gopalakrishnan et al. does not teach the step of enlarging the spacing as many times as is enlargeable

9. Examiner respectfully disagrees for the following reasons:

As to a) Gopalakrishnan et al. teaches an ability of the compaction method of **increasing** the spacing or distance between member devices (col. 6, l.67; col. 7, ll.1-2), wherein increasing the spacing between members is performed, when a **violation of spacing constraint is found** as a result of compaction the layout of IC (col. 3, ll.35-47), and increasing the space between member devices is **de-compacting** to overcome the violation of the spacing constraint (col. 3, ll.44-47); and by performing decreasing the

distance between member devices iteratively (col. 7, ll.38-42) until the spacing constraints are met (col. 14, ll.50-53).

As to b) Gopalakrishnan et al. teaches increasing the space between member devices as de-compacting the layout to overcome the violation of the spacing constraint (col. 3, ll.44-47), wherein spacing constraint sets a minimum distance between member devices (abstract).

As to c) Gopalakrishnan et al. teaches performing decreasing the distance between member devices iteratively (col. 7, ll.38-42) until the spacing constraints are met (col. 14, ll.50-53).

Examiner maintains the rejection of claims 1-6, 8-10 under 35 USC § 102.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Helen Rossoshek whose telephone number is 571-272-1905. The examiner can normally be reached on 7:30-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Examiner
Helen Rossoshek
AU 2825

A. M. Thompson
Primary Examiner
Technology Center 2800